WHAT IS CLAIMED IS:

1. A field-effect-type semiconductor device comprising:

a channel region of a first conduction-type semiconductor;

a first-conduction-type emitter region being in contact with the channel region, and being a first conduction type semiconductor with higher concentration than that of the channel region;

a gate electrode penetrating the channel region, and insulated from the channel region and the first-conduction-type emitter region; and

an emitter electrode being in contact with the channel region and with the first-conduction-type emitter region.

2. A field-effect-type semiconductor device according to claim 1 further comprising a second-conduction-type emitter region being insulated from the gate electrode, the second-conduction-type emitter region being a second conduction-type semiconductor,

wherein the second-conduction-type emitter region is in contact with the channel region and the emitter electrode, and

the gate electrode faces the second-conduction-type emitter region, the channel region and a contact portion of those regions.

3. A field-effect-type semiconductor device according

to claim 1, wherein gate electrodes are formed linearly, and channel regions are formed discretely between adjoining gate electrodes at surface level.

4. A field-effect-type semiconductor device according to claim 2, wherein gate electrodes are formed linearly, and channel regions are formed discretely between adjoining gate electrodes at surface level.

5. A field-effect-type semiconductor device according to claim 3, wherein a width of a channel section in which the second-conduction-type emitter region and the channel region are in contact with each other at a face facing the gate electrode is narrower than an interval between adjoining channel sections.

6. A field-effect-type semiconductor device according to claim 4, wherein a width of a channel section in which the second-conduction-type emitter region and the channel region are in contact with each other at a face facing the gate electrode is narrower than an interval between adjoining channel sections.

7. A field-effect-type semiconductor device according to claim 2, wherein gate electrodes are formed linearly, second-conduction-type emitter regions are formed discretely between adjoining gate electrodes, and each second-conduction-type emitter region is facing

adjoining two gate electrodes.

8. A field-effect-type semiconductor device according to claim 7, wherein the first-conduction-type emitter region is formed between adjoining two second-conduction-type emitter regions with its width being narrower than a width of the emitter electrode.

9. A field-effect-type semiconductor device according to claim 8, wherein, in an area at surface level between two adjoining second-conduction-type emitter regions, a portion other than the first-conduction-type emitter region is occupied by the channel region.

10. A field-effect-type semiconductor device according to claim 7, wherein first-conduction-type emitter regions are formed discretely between adjoining gate electrodes, and
each first-conduction-type emitter region is facing adjoining two gate electrodes.

11. A field-effect-type semiconductor device according to claim 10, wherein an area at surface level between a second-conduction-type emitter region and a first-conduction-type emitter region that adjoin to each other is occupied by the channel region.

12. A field-effect-type semiconductor device according

to claim 7 further comprising a drift region arranged below the channel region, the drift region being a second conduction-type semiconductor,

wherein a part of an area at surface level surrounded by adjoining second-conduction-type emitter regions and adjoining gate electrodes is occupied by the drift region.

13. A field-effect-type semiconductor device according to claim 8 further comprising a drift region arranged below the channel region, the drift region being a second conduction-type semiconductor,

wherein a part of an area at surface level surrounded by adjoining second-conduction-type emitter regions and adjoining gate electrodes is occupied by the drift region.

14. A field-effect-type semiconductor device according to claim 12, wherein pluralities of contact opening in which the emitter electrode is in contact with the channel region, the first-conduction-type emitter region and the second-conduction-type emitter region are arranged discretely avoiding the drift region.

15. A field-effect-type semiconductor device according to claim 13, wherein pluralities of contact opening in which the emitter electrode is in contact with the channel region, the first-conduction-type emitter region and the second-conduction-type emitter region are arranged discretely avoiding the drift region.

16. A field-effect-type semiconductor device according to claim 2, wherein

gate electrodes are formed insularly,

the second-conduction-type emitter region is arranged between adjoining gate electrodes, and

areas at surface level surrounding gate electrodes are occupied by the channel region except for a part that is occupied by the second-conduction-type emitter region.

17. A field-effect-type semiconductor device according to claim 5, wherein

gate electrodes are formed insularly,

the second-conduction-type emitter region is arranged between adjoining gate electrodes, and

areas at surface level surrounding gate electrodes are occupied by the channel region except for a part that is occupied by the second-conduction-type emitter region.

18. A field-effect-type semiconductor device according to claim 16, wherein the first-conduction-type emitter region is formed between adjoining two second-conduction-type emitter regions with its width being narrower than a width of the emitter electrode.

19. A field-effect-type semiconductor device according to claim 17, wherein the first-conduction-type emitter region is formed between adjoining two

second-conduction-type emitter regions with its width being narrower than a width of the emitter electrode.

20. A field-effect-type semiconductor device according to claim 16 further comprising a drift region arranged below the channel region, the drift region being a second conduction-type semiconductor,

wherein a part of an area at surface level surrounded by adjoining second-conduction-type emitter regions and adjoining gate electrodes is occupied by the drift region, and

pluralities of contact opening in which the emitter electrode is in contact with the channel region, the first-conduction-type emitter region and the second-conduction-type emitter region are arranged discretely avoiding the drift region.